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JAPANESE PATENT OFFICE
PATENT JOURNAL (A)
KOKAI PATENT APPLICATION NO. HEI 6[1994]-61417

BA
SCOPE
RECEIVED
JAN 14 2003
TECHNOLOGY CENTER 2800

Int. Cl.⁵: H 01 L 25/04
25/18

Filing No.: Hei 4[1992]-242753

Filing Date: August 19, 1992

Publication Date: March 4, 1994

No. of Claims: 17 (Total of 13 pages)

Examination Request: Not filed

SEMICONDUCTOR DEVICE, ELECTRONIC CIRCUIT DEVICE, AND
MANUFACTURING METHODS AND MANUFACTURING APPARATUS
THEREFOR

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[Attached amendments have been incorporated into text of translation.]

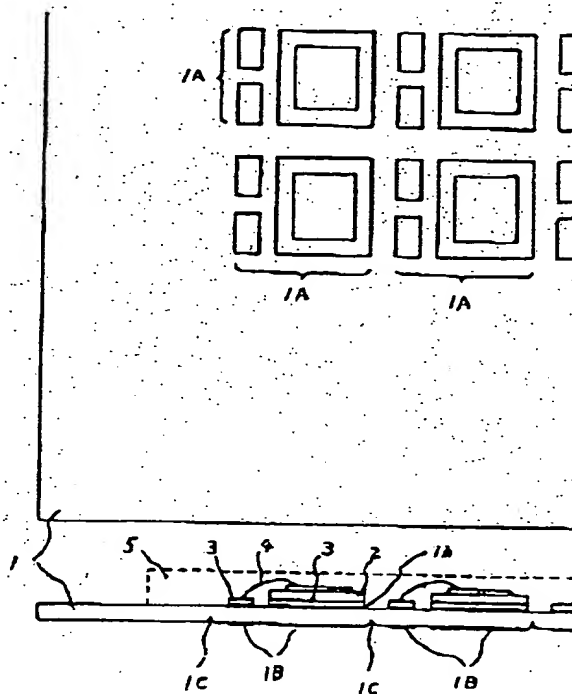
Abstract

Objective

The objective of the present invention is to provide a semiconductor device that is small, thin, lightweight, and can be sealed with an inexpensive resin, as well as small power sources and other electronic circuit devices, using simple and inexpensive equipment.

Constitution

The invention comprises a large-area electrically insulated substrate, on which is formed plural prescribed electroconductive patterns on one principal surface and plural scribe lines that do not affect said prescribed electroconductive patterns on the other principal surface; one or more circuit elements fixed to each of said prescribed electroconductive patterns; a sealing resin that seals the entire surface of the portion where said electroconductive patterns are formed on said large-area electrically insulated substrate; and grooves formed to a prescribed depth along sites corresponding to said scribe lines.



Claims

1. A semiconductor device characterized by the following facts: the semiconductor device has a sealing resin for sealing one or more semiconductor elements fixed to the prescribed electroconductive pattern formed on one principal surface of an electrically insulated substrate, wherein said sealing resin has a flat upper surface almost equal in size to the area of the principal surface of said electric insulating substrate, and a molding side wall surface that extends almost vertically from the periphery of said electric insulating substrate to said upper surface.

2. A semiconductor device characterized by the following facts: the semiconductor device has a sealing resin for sealing one or more semiconductor elements fixed to the prescribed electroconductive pattern formed on one principal surface of an electrically insulated substrate, wherein said sealing resin has a smooth upper surface almost equal in size to the area of the principal surface of said electric insulating substrate, and a molding side wall surface that extends almost vertically from the periphery of said electric insulating substrate to said upper surface and that is rougher than said smooth upper surface.

3. A large-area semiconductor device characterized by the fact that it comprises the following parts: a large-area electrically insulated substrate, on which is formed plural prescribed electroconductive patterns on one principal surface and plural scribe lines that do not affect said

prescribed electroconductive patterns on the other principal surface; one or more circuit elements fixed to each of said prescribed electroconductive patterns; a sealing resin that seals the entire surface of the portion where said electroconductive patterns are formed on said large-area electrically insulated substrate; and grooves formed with a prescribed depth along sites corresponding to said scribe lines.

4. The large-area semiconductor device described in Claim 3 characterized by the fact that the bottom of said groove reaches the surface of said large-area electrically insulated substrate.

5. The large-area semiconductor device described in Claim 3 characterized by the following facts: the distance between the bottom of said groove and the surface of said large-area electrically insulated substrate is about 2 mm or less; and said scribe lines are formed on the surface of said large-area electrically insulated substrate on the side opposite the side where the sealing resin is present.

6. A large-area semiconductor device characterized by the fact that it comprises the following parts: a large-area electrically insulated substrate, on which is formed plural prescribed electroconductive patterns on one principal surface and plural scribe lines that do not affect said prescribed electroconductive patterns on the other principal surface; one or more circuit elements fixed to each said prescribed electroconductive patterns; and a sealing resin that seals the entire surface of the portion where said electroconductive patterns are formed on said large-area electrically insulated substrate and has a thickness of 2 mm or less.

7. The semiconductor device described in any of Claims 1-6 as a surface-mounting device, characterized by the fact that another prescribed electrode pattern is formed on the other principal surface of said electrically insulated substrate, and it is connected through via holes to the prescribed electroconductive pattern formed on said one principal surface of said electrically insulated substrate.

8. The semiconductor device described in any of Claims 1-7 as a surface-mounting device, characterized by the fact that said semiconductor element has different electrodes on said principal surface, wherein said electrodes are fixed to independent electroconductive films of the electroconductive pattern.

9. The electronic circuit device described in any of Claims 1-8 characterized by the fact that in addition to said semiconductor element, there are other circuit elements that are electrically connected to said electroconductive pattern.

10. A semiconductor device manufacturing method characterized by the following facts: a large-area electrically insulated substrate, on which is formed plural prescribed electroconductive patterns on one principal surface and plural scribe lines formed on at least one principal surface such that they do not affect said prescribed electroconductive patterns, is

prepared; after one or more semiconductor elements are fixed to each of said prescribed electroconductive patterns, the entire surface of the portion of said large-area electrically insulated substrate on which said electroconductive pattern is formed is completely sealed with a sealing resin such that the sealing resin has a flat surface; during the curing of the sealing resin, an external force is applied to divide said electrically insulated substrate and the sealing resin along said scribe lines to produce individual semiconductor devices.

11. The semiconductor device manufacturing method described in Claim 10 characterized by the fact that the division is performed when said sealing resin is in a half-cured state at a temperature below 80% of the thermal deformation temperature when said sealing resin is fully cured.

12. The semiconductor device manufacturing method described in Claim 10 or 11 characterized by the fact that further heating for curing is performed after dividing to form individual semiconductor devices.

13. A semiconductor device manufacturing method characterized by the following facts: a large-area electrically insulated substrate, on which is formed plural prescribed electroconductive patterns on one principal surface and plural scribe lines formed on at least one principal surface such that they do not affect said prescribed electroconductive patterns, is prepared; after one or more semiconductor elements are fixed to each of said prescribed electroconductive patterns, the entire surface of the portion of said large-area electrically insulated substrate on which said electroconductive pattern is formed is entirely sealed with a sealing resin such that the sealing resin has a flat surface; at the same time, grooves are formed to a prescribed depth along the sites of said sealing resin corresponding to said scribe lines; then, heat-curing is performed, and an external force is applied to divide said electrically insulated substrate and sealing resin along said scribe lines to produce individual semiconductor devices.

14. The semiconductor device manufacturing method described in Claim 13 characterized by the fact that a casting mold, which has narrow ridges with a prescribed height formed along the sites corresponding to said scribe lines on a flat surface, is prepared, and, by means of the narrow ridges with a prescribed height, grooves are formed to a prescribed depth along the sites of said sealing resin corresponding to said scribe lines.

15. A semiconductor device manufacturing method characterized by the following facts: a large-area electrically insulated substrate, on which plural prescribed electroconductive patterns are formed on one principal surface and plural scribe lines are formed on at least one principal surface such that they do not affect said prescribed electroconductive patterns, is prepared; after one or more semiconductor elements are fixed to each of said prescribed electroconductive patterns, a radiation-curable resin is applied to cover the entire surface of the portion of said large-area electrically insulated substrate where said electroconductive pattern is

formed, such that a flat surface is formed; then, a casting mold, which is made of a transparent material and has plural ridges of prescribed height along the sites of said radiation-curable resin with active energy radiation corresponding to said scribe lines, is pressed against the resin that can be cured with active energy radiation; and radiant energy is then passed through said casting element so as to cure the radiation-curable resin.

16. The electronic circuit device manufacturing method described in any of Claims 10-15 characterized by the fact that in addition to said electroconductive element, there are other circuit elements that are electrically connected to said electroconductive pattern.

17. A semiconductor device manufacturing apparatus characterized by the fact that it is composed of the following parts: a casting mold for a large-area electrically insulated substrate that plural prescribed electroconductive patterns formed on one principal surface and has plural scribe lines formed on at least one principal surface such that they do not affect said prescribed electroconductive patterns, where said mold comprises a frame portion that fits the large-area electrically insulated substrate having one or more semiconductor elements fixed to each of said prescribed electroconductive patterns; and a press-casting mold element, which is made of transparent material, has plural ridges of prescribed height along sites corresponding to said plural scribe lines, and through-holes for the escape of excess sealing resin.

Detailed explanation of the invention

[0001]

Industrial application field

The present invention pertains to a semiconductor device that is small, lightweight, and thin, and is appropriate for surface mounting, and has semiconductor elements fixed to an electroconductive pattern on an electrically insulated substrate sealed with a resin, as well as an electronic circuit device, and their manufacturing methods.

[0002]

Prior art

There is a great demand for the miniaturization of power converters, etc. As a result, on-board power sources (OBP), etc. that can be surface-mounted have been developed. However, when a large converter is to be formed as a small-size OBP, because some of the semiconductor elements used in it are too large, it is impossible to keep the overall size of the device small, which is disadvantageous. In particular, since Schottky barrier diodes, bipolar transistors, MOSFETs, and other semiconductor elements of relatively large size liberate significant amounts of heat, a metal heat sink with external leads is placed in the transfer mold in order to

increase the heat dissipation effect. However, this increases the size of the device, and it is thus difficult to keep the overall size of the system carried on the substrate small.

[0003]

If semiconductor elements such as paired chips of said Schottky barrier diodes, bipolar transistors, MOSFETs, and other semiconductor elements can be directly mounted on a substrate, bonded, and molded, they are good candidates for miniaturization. However, relatively large semiconductor devices have low impact-resistance, moisture-resistance, and other features pertaining to reliability, and are associated with other disadvantages. Also, many circuit devices are resin-sealed surface-mounted devices. If some of them are paired chips, they should be separated for mounting, and treated in different processing steps. As a result, expensive dedicated devices are needed, and the number of manufacturing steps is increased. The cost rises, which is disadvantageous. Also, the following method may be adopted for mounting semiconductor elements: the aforementioned semiconductor elements are attached by soldering to an alumina substrate or the like with excellent heat dissipation, and wire bonding to the electrode pads, etc. is performed. Then, a sealing resin is poured. On the inner surface of the substrate, electrodes are formed and they are conducted through via holes. Consequently, it is appropriate for miniaturization. However, the cured sealing resin is molded to have the form of a convex lens. This non-planar shape therefore cannot be used in automatic mounting by means of suction under reduced pressure.

[0004]

In addition to improved quality, surface-mount devices are required to be small, thin, lightweight, and inexpensive. Usually, capacitors, resistors, coils, transformers, IC, diodes, transistors, and other circuit devices are designed to have shapes that allow easy mounting on a substrate. The circuit devices are mounted on the substrate surface using a high-speed automatic inserting machine. In this method, solder cream is coated at the prescribed positions of the electroconductive pattern on the substrate. Then, the circuit devices are carried and bonded temporarily, followed by soldering by means of reflow heat treatment or the like. In the surface mounting method, since the circuit devices are held under reduced pressure and carried, naturally it is preferred that they be lightweight and flat. Also, in order to maintain the quality, packing is performed using an epoxy resin or another resin with excellent electrical insulation, and transfer molding or the like is used for series production.

[0005]

The surface mount semiconductor device of the general lead wire type shown in Figure 10 will be examined. Semiconductor element (52) is soldered to the flat substrate surface using the ends of a pair of lead electrodes (50), (51), which are bent so that they form a flat surface. By means of internal lead terminal (53), said semiconductor element (52) is connected to lead electrode (51) on the other side, and the flat portions of lead electrodes (50), (51) and semiconductor element (52) are molded with sealing resin (54). Also, in order to realize a small, thin shape and to reduce the number of man-hours required for processing, paired chip or flip-chip may be directly mounted on the electroconductive pattern of the substrate using the die bonding method or another method, and, bonding to an electroconductive pattern containing electrodes and wiring pattern is performed and an epoxy resin with good insulating property is dripped for coating. This method is described, for example, in Japanese Kokai Patent Application No. Sho 62[1987]-208652. As illustrated in Figure 11, first, die bonding material (62) is used to bond semiconductor element (63) [sic] to substrate (61), and electrical connection is performed by means of fine metal wires (63). Then, casting element (66) is pressed on dam (65), and sealing resin (67) is injected into the package through groove (64) of dam (65). Then, after the curing of sealing resin (67), casting element (66) is removed, and a resin-sealed semiconductor device is produced.

[0006]

Problems to be solved by the invention

However, in the semiconductor device shown in Figure 10, the pair of lead electrodes (50), (51) are bent into an L. Consequently, it is difficult to make the device thin, which is a significant problem. Also, in this case, it is necessary to perform transfer molding for each device, including a portion of a pair of lead electrodes (50), (51). Consequently, a special transfer molding device is required, and it is difficult to series-produce. In addition, because the pair of lead electrodes (50), (51) are bent into an L, it is difficult to miniaturize. In the case shown in Figure 11, when resin sealing is to produce a flat upper surface, it is necessary to have a step in which casting element (66) is pressed on each dam (65), and sealing resin (67) is injected from groove (64) of dam (65) into the package. Consequently, this method is not used for series production. Also, the size of the substrate must be increased to correspond to the area of dam (65). Thus, there is also the problem related to miniaturization. Also, although not shown in the figure, for a semiconductor device for power use and having lead wires extending from the sealing resin, after resin sealing, it is necessary to perform plural burr removing steps of operation, including removal of burr for the root portion of the lead wires, and it is difficult to miniaturize the semiconductor device. The purpose of the present invention is to provide a

manufacturing method for semiconductor devices, comprising Schottky barrier diodes, bipolar transistors, MOSFETs, and other semiconductor elements of relatively large size, in a package which is small, flat, thin, and lightweight, and can be series-produced, and has high heat-resistance, high moisture-resistance, good reliability in PCT tests, and other excellent characteristics.

[0007]

Means to solve the problems

In order to solve the aforementioned problems, the first portion of the present invention provides a method characterized by the following facts: a large-area electrically insulated substrate, on which is formed plural prescribed electroconductive patterns on one principal surface and plural scribe lines that do not affect said prescribed electroconductive patterns on the other principal surface, is prepared; after circuit elements are fixed to each of said prescribed electroconductive patterns, a sealing resin is applied to seal the entire surface of the portion where said electroconductive patterns are formed on said large-area electrically insulated substrate; grooves with a prescribed depth are formed along the sites corresponding to the aforementioned scribe lines of said sealing resin, as required. The second portion of the invention provides a method characterized by the following facts: a large-area electrically insulated substrate, which has plural prescribed electroconductive patterns on one principal surface and plural scribe lines formed on at least one principal surface such that they do not affect said prescribed electroconductive patterns, is prepared; after one or more semiconductor elements are fixed on each of said prescribed electroconductive patterns, the entire surface of the portion of said large-area electrically insulated substrate with said electroconductive pattern formed on it is entirely sealed with a sealing resin such that the sealing resin has a flat surface; during the curing of the sealing resin, an external force is applied to divide said electrically insulated substrate and the sealing resin along said scribe lines to produce individual semiconductor devices and electronic circuit devices.

[0008]

Application examples

Figure 1 illustrates an application example of the present invention. Figure 1 shows an example of transistor. (1) represents a large-area electrically insulated substrate made of inorganic alumina, aluminum nitride, glass, a ceramic, aluminum, copper, or other metal plates with an insulating film made of polyimide or the like bonded to it. On one principal surface, prescribed electroconductive patterns (1A) are formed in a regular matrix configuration. On the other principal surface, electrode patterns (1B) corresponding to said electroconductive patterns

(1A), respectively, are formed. Electroconductive patterns (1A) and electrode patterns (1B) are connected as desired through conventional via holes, not shown in the figure. Said electroconductive patterns (1A) and electrode patterns (1B) are formed by silk-screen printing an electroconductive paste made of copper, tungsten or the like, followed by baking for attachment to form electrodes for transistors. Electrode patterns (1B) function as external electrodes attached by soldering to a printed board or another printed circuit pattern not shown in the figure. Also, lattice-shaped scribe lines (1C) are formed on the surface where electrode patterns (1B) are formed and/or the other surface, in such a way that they do not affect electroconductive patterns (1A) and electrode patterns (1B). Said scribe lines (1C) are formed to facilitate cutting the large-area molding to be performed later. They may be mechanically formed V-shaped grooves, or shallow fissures formed along the desired lines under the action of ultrasound, or the like, or lines formed to have low strength. Other than grooves, the scribe lines usually cannot be seen.

[0009]

Then, semiconductor elements (2) are attached by means of solder layer (3) to the prescribed portions of electroconductive patterns (1A). Then, by means of wire-bonding of metal wires (4), the emitter electrodes and base electrodes of the transistors are connected to the prescribed portions of electroconductive patterns (1A). The next processing step (not shown in the figure) is to apply polyimide varnish or another precoating resin for conventional passivation. Then, prescribed sealing resin (5) is used to seal all of electroconductive patterns (1A) and semiconductor elements (2) uniformly, followed by division to form individual semiconductor devices. In this case, since scribe lines (1C) are formed on the principal surface of the large-area electrically insulated substrate on the side opposite to the surface covered with sealing resin (5), division can be performed easily. On the other hand, if scribe lines (1C) are formed only on the surface covered with sealing resin (5), it is very difficult to perform division. In the example shown in Figure 1, electroconductive pattern (1A) and electrode pattern (1B) are for discrete semiconductor element (2). However, it is also easy to use electroconductive pattern (1A) and electrode pattern (1B) to form a hybrid integrated circuit, power source circuit, or another circuit constitution carrying at least one semiconductor element and at least one other active element and passive element. After said elements are carried and bonded for the prescribed connection, they are also sealed off uniformly, followed by division to form individual electronic circuit devices.

[0010]

In the following, let's look at the resin sealing operation in more detail. First sealing resin (5) is prepared from epoxy resin, phenolic resin, polyester resin, or another electrically insulated

resin. The thermosetting resin resins that can be cured gradually under heat are preferred. For reasons that will be explained below, it is appropriate to use a resin (in particular, epoxy resin) that goes through half-curing or B-stage state as a base resin. As curing agent and catalyst, one may make use of acid anhydride, phenolic resin, aromatic amine, imidazole, etc. Also, one may add pigments, fillers, additives, etc. for maintaining the desired characteristics. Examples of fillers that may be added include quartz powder, alumina, etc. Usually, the proportion may be 60% or higher. Also, it is required to have good adhesiveness with electrically insulated substrate (1), dividing property, mold release property, fluidity, low-temperature curing property, defoaming property, low thixotropy, and other operation properties, as well as low expansion, low concentration of impurity, etc. As the thermoplastic resin, one may make use of PPO and liquid crystal polymer. However, it is necessary to melt it and inject the melt.

[0011]

The following is a specific example of the epoxy resin based sealing resin.

Epichron [transliteration] #850 (product of Dai-Nippon Ink Chemical Co., Ltd.):	15 parts
Chissonox #221 (product of Nippon Chisso K.K.):	10 parts
Chissonox #221 (product of Nippon Chisso K.K.):	10 parts [sic]
Reactive diluent Gan (product of Nippon Kayaku K.K.):	5 parts
Fuserex [transliteration] Y-60 (product of Tatsumori K.K.):	133 parts
EPICHRON #B-4136 (product of Dai-Nippon Ink Chemical Co., Ltd.):	27 parts
1B2MZ (product of Shikoku Kasei K.K.):	0.5 part
Defoaming agent (TSA-750, product of Toshiba Silicone Co., Ltd.):	0.01 part
total	200.51 parts

The above-listed composition was well agitated with an agitator, followed by defoaming in vacuum.

[0012]

In the following, let's look at the method for forming a molding of the sealing resin with a flat upper surface by means of the sealing resin treated as follows. As explained above, as shown in Figure 2, after semiconductor elements (2), etc. are covered with polyimide varnish or another precoating resin, large-area electrically insulated substrate (1) is placed in upper casting element (6) in the form of a frame and with a height of 5 mm, and plate-shaped lower casting element (7), so that there is no leakage of the sealing resin. In this case, the casting element is not limited to metal. One may also use rubber, plastic, and other materials. Also, in order to improve the mold-release property, the mold-release treatment may be performed, or a mold of silicone resin

may be used. As required, one may also perform sealing and packing treatment free of resin leakage, and make use of a pressurizing mechanism to apply the necessary pressure.

[0013]

After the peripheral portion of large-area electrically insulated substrate (1) is held between upper casting element (6) and lower casting element (7), as explained above, a liquid sealing resin is fed into the entire surface inside the frame until the thickness becomes 1.5 mm. Then, the unit is loaded in a vacuum device (not shown in the figure) for vacuum defoaming. In this way, since the air in the sealing resin is removed beforehand, the defoaming time during sealing can be shortened. Here, "vacuum" means a vacuum level as low as 100 mmHg prepared by reducing the pressure to enable removal of air from the sealing resin. The liquid sealing resin can be injected at atmospheric pressure or vacuum. Of course, one may also perform vacuum defoaming after injection of the undefoamed resin. If such a defoaming operation is not performed, usually, bubbles remain on the surface of the sealing resin. Then, the casting element is kept horizontal, and vacuum defoaming is performed at a vacuum of 2 mmHg for 5 min, followed by heating for curing at 160° for about 2 h. After casting elements (6) and (7) are removed, an external force is applied along scribe lines (1C) on the inner surface of electrically insulated substrate (1) to divide the molded product into plural individual semiconductor devices. In this case, the heating curing temperature depends on the type of sealing resin. During transfer molding, the temperature of the casting element is in the range of 180-250°C for a time of 2-10 min. These conditions are appropriate for series production. Also, the injection method is performed at a temperature in the range of 80-180°C for a time in the range of 10 min to 2 h.

[0014]

When the thickness of sealing resin (5) is about 2 mm or less, it is easy to use a manual operation to divide the semiconductor devices along scribe lines (1C) without any adverse influence on the semiconductor elements, etc. When the thickness of sealing resin (5) is greater than about 2 mm, as shown in Figure 3, one may form grooves (5A) with a concave shape, linear shape, or V-cut shape at sites corresponding to scribe lines (1C) on the inner surface of electrically insulated substrate (1). For grooves (5A) formed in grid configuration, the thickness from the bottom of the groove to the surface of electrically insulated substrate (1) is about 2 mm or smaller. Also, the thickness of sealing resin (5) depends on the particular semiconductor device, power source, and other electronic circuit device, and it is usually in the range of 1-5 mm. When it is rather thick, the upper surface of the large-area molding may deform, and the electrical characteristics may be adversely affected. Consequently, by forming grooves (5A) in grid form at sites of sealing resin (5) corresponding to scribe lines (1C) on the inner surface of

electrically insulated substrate (1), it is possible to obtain a flat large-area molded product with relatively little deformation.

[0015]

Because the large-area molded product is formed with the sealing resin cast on almost the entire surface of electrically insulated substrate (1), its upper surface is smooth. Thus, naturally, the upper surface of the divided semiconductor devices will also be smooth. However, the side wall surface formed by dividing along grooves (5A) is rougher than the upper surface, and this indicates that division can be performed easily. As a simple method of forming grooves (5A) on the large-area molding, as shown in Figure 4, press-casting element (8) is used to press sealing resin (5) before it is cured, and a liquid sealing resin is fed between upper casting element (6) and lower casting element (7) with press-casting element (8) preset. This press-casting element (8) has a surface with protruding portions, that is, ridges (8A), formed in a grid with the same spacing as scribe lines (1C) of electrically insulated substrate (1). The portion surrounded by ridges (8A) is lower than ridges (8A). The shape and height of ridges (8A) correspond to grooves (5A) to be formed. The material for making press-casting element (8) is the same as that of upper casting element (6) and lower casting element (7). In this case, in order to perform resin sealing in an appropriate way, one may form location, (not shown in the figure) for the escape of excess sealing resin when the sealing resin is pressed by the press-casting element between said upper casting element and press-casting element. In addition, when the press-casting element is set in vacuum, it is possible to obtain a smooth surface with few bubbles. Also, if required, one may form a pattern on the surface of the casting element to stamp a mark, etc.

[0016]

In the following, examples of the resin sealing-method will be examined.

Example 1

As shown in Figure 1, plural paired chip semiconductor elements (2) having relatively high current capacity are set on a 0.4-mm-thick electrically insulated substrate (1) made of alumina with plural printed electroconductive patterns (1A). The obtained unit is set in the casting element. At the same time, the thickness of the sealing resin is set to 1 mm. By means of a transfer mold device, a transfer molding resin MP-3000 (product of Nitto Denko K.K.) is heated and melted, and the melt is injected over the entire surface inside the casting element. Then, heat-curing is performed for 2 min with the casting element at 180°C. When the cured molded product is removed from the frame of the casting element, a large-area molded product with the entire surface sealing resin (5) flat, as shown in Figure 5, is obtained. Dividing along

scribe lines (1C) formed on the inner surface of electrically insulated substrate (1), forms semiconductor devices with a smooth upper surface and four rough side wall surfaces. Compared with conventional elements of the same current capacity, the obtained semiconductor devices have an assembly area smaller by a factor in the range of $1/3$ - $1/4$ and a thickness smaller by a factor of $1/2$ or less. That is, it is significantly miniaturized.

[0017]

Example 2

At a position opposite the scribe lines formed on the inner surface of a 0.635-mm-thick electrically insulated substrate made of alumina and having prescribed circuit elements placed on plural circuit patterns of the same type, as shown in Figure 3, the casting element that provides V-shaped grooves with a depth of about 2 mm is positioned as shown in Figure 4, such that the thickness of the sealing resin is 4 mm. The sealing resin of the aforementioned composition example is injected into the casting elements to form a molded product with a thickness of 4 mm of the sealing resin. It is heated with the casting element at 150°C for 10 h. After curing, the cured molded product is removed from the frame of the casting element. As shown in Figure 3, a large-area molded product with grooves (5A) formed in a grid on the surface of sealing resin (5) is obtained. When dividing is performed along said grid-shaped grooves (5A), resin-sealed electronic circuit devices with a smooth upper surface and four divided side wall surfaces that are rougher than the upper surface are obtained. The initial electrical characteristics of the electronic circuit devices obtained in this way can be maintained, and there is no adverse influence from the resin sealing or mechanical division. That is, high-quality electronic circuit devices can be produced. Compared with conventional electronic circuit devices of the same type, the aforementioned electronic circuit devices have an assembly area smaller by a factor of $1/3$ - $1/4$ and thickness smaller by a factor of about $1/2$. That is, the devices are much smaller and are lighter in weight. For the obtained resin sealed semiconductor devices and resin sealed electronic circuit devices, there is no need to perform burr removal.

[0018]

In the application example described above, after the sealing resin fully cures, the large-area molded product is divided. However, one may also adopt the following method: a heat-setting resin that goes through a half-curing stage or a B stage is used as the sealing resin; and, when the sealing resin is in the half-cured state (about 90% or lower the fully cured state) during the heat-setting process, heating is stopped, and division is performed. In this case, division can be performed with an external force much smaller than that required for division of the sealing resin after curing. In this application example, as explained above, plural

semiconductor elements, resistors, capacitors, inductors, and other circuit members (some of which are of the paired chip type) are mounted and fixed on electrically insulated substrate (1) made of alumina with plural circuit patterns and, the prescribed connections are performed to form a power source circuit. Then, it is placed in a mold made of silicone rubber with height of 2 mm and bonded. The epoxy-based sealing resin in the aforementioned composition example is injected over the entire surface to a height of 2 mm, and vacuum defoaming is carried out while the unit is heated at 120°C at atmospheric pressure for 15 min form a half-cured, large-area molded product. The thermal deformation temperature at the time of complete curing of the sealing resin 165°C. In this case, the thermal deformation temperature in the half-cured state is 72°C. Then, the silicone rubber mold is removed, and a flat large-area molded product with height of 2 mm of the sealing resin is obtained. One may simply divide along the scribe lines on the inner surface of electrically insulated substrate (1).

[0019]

In the following, several examples will be examined.

Example 1

As shown in Figure 1, plural semiconductor elements (2) were mounted on 0.5-mm-thick electrically insulated substrate (1) made of alumina with plural printed electroconductive patterns (1A). Then, it is placed between an upper casting element and a lower casting element separated by 3 mm. Then, a liquid epoxy resin was injected over the entire surface inside the casting elements until it overflowed to form a molded product 3 mm thick. Then, vacuum defoaming was performed at 758 mmHg for 10 min, followed by heating at 80°C for 60 min to realize half-curing. The thermal deformation temperature at the time of full curing of the resin is about 165°C, and the thermal deformation temperature in the half-cured state is 64°C. The obtained large-area molded product with a height of 3 mm of the resin with a flat surface is almost free of deformation, and it is possible to easily divide it along scribe lines (1C) on the inner surface of electrically insulated substrate (1). Then, the divided individual semiconductor devices were heated to about 150°C for about 20 h to realize full curing. The side wall surfaces of the divided semiconductor devices are rougher than the smooth upper surface, but the cuts along scribe lines (1C) are clean, and it high-quality semiconductor products can be produced.

[0020]

Example 2

At a position opposite the scribe lines formed on the inner surface of a 0.4-mm-thick electrically insulated substrate made of alumina and having prescribed circuit members mounted

on plural circuit patterns of the same type, as shown in Figure 3, the casting element that provides V-shape grooves with a depth of about 1 mm was positioned as shown in Figure 4, such that the thickness of the sealing resin is 3 mm. The sealing resin of the aforementioned composition example, that is, an epoxy/acid anhydride/imidazole-based sealing resin containing 70% silica powder, was injected into the casting elements to form a molded product with thickness of 3 mm of the sealing resin. It was heated with the casting element to 160°C for 10 min for half-curing. In the half-cured state, the large-area molded product was removed from the casting element frame. Compared with Example 1, the deformation of the large-area molded product is a little smaller, and it is even easier to divide along grid-like grooves (5A). Also, while the thermal deformation temperature in full curing state of the resin is 165°C, the thermal deformation temperature in the half-cured state is 130°C. For all of the semiconductor devices obtained in this way, the initial electrical characteristics are maintained, and no adverse influence of the resin sealing or mechanical division was observed. Tests were also performed on the division of other sealing resins in the half-cured state. The results for the sealing resin used in the aforementioned application example in the half-cured state at a temperature less than 80% of the thermal deformation temperature for full curing, indicated that it is preferred to divide the molded product in the half-cured state at a temperature of 50% of the temperature for full curing or lower. Also, in this case, during division, the mechanical stress is low, and heat-curing is performed at a temperature below that for full curing. Consequently, mechanical stress during curing of the sealing resin is also low, and, it is possible to significantly reduce the influence on the semiconductor elements and other circuit elements.

[0021]

In the aforementioned application example, a type of heat setting resin was used. In the following, let's look at the method and device for manufacturing semiconductor devices and electronic circuit devices using UV-curable resin, electron-beam curable resin, and other radiation-curable resins. First of all, let's look at the typical composition for a resin that can be cured with active energy radiation. The resin composition may contain alkyd resins, urethane resins, polyurethane resins [sic], epoxy resins, etc. for introducing acrylate groups, allyl groups, itaconate groups, conjugated double bonds and other unsaturated groups. Other components include oligomers monomers and other viscosity adjusting agents, as well as photopolymerization initiating agents, heat setting catalysts, etc. In addition, one may add conventional types of pigments, dyes, fillers, and additives. Also, one may add as required, heat-setting resins, and other resins that barely react to active energy radiation. The following is a specific example of the composition of a UV-curable resin.

Goseilac [transliteration] UV-7000B

(product of Nippon Gosei Kagaku Kogyo K.K.):	66 parts by weight
TMPTA (trimethylpropane triacrylate):	30 parts by weight
Irgacure 651 (product of Ciba Geigy Co.):	4 parts by weight

Total: 100 parts by weight

[0022]

In the following, a manufacturing device for forming plural resin sealing portions on the surface of large-area electrically insulated substrate (1) as described in the aforementioned application example using the above listed composition of UV curable resin will be examined, with reference to Figure 6. Figures 6(A) and (B) are a front view and a side view of press-casting element (8) that forms a portion of the manufacturing device. It is made of silicone resin, acrylic resin, or another plastic resin, or glass or another transparent material. Press-casting element (8) is composed of base portion (8A) and pressing portion (8B). Pressing portion (8B) has pressing surface (8B1) that is almost the same size as the surface surrounded by the inner wall of upper casting element (6) in the frame shape as shown in Figure 6(C). On its pressing surface (8B1), grid-like ridges (8B2) with a V-shaped cross-section of the pattern corresponding to the grid-shaped scribe lines formed on large-area electrically insulated substrate (1) are formed. The height of ridges (8B2) depends on the thickness of the sealing resin formed on large-area electrically insulated substrate (1). That is, the thickness of the sealing resin is almost equal to the height of ridges (8B2). Also, through-holes (8B3) are formed at the four corners of pressing element (8B) for the excess sealing resin to escape. Said through-holes (8B3) are formed connected to through-holes (8A1) formed on base portion (8A).

[0023]

As shown in Figure 6(C), for upper casting element (6), portion (6A) that is almost equal to the thickness of large-area electrically insulated substrate (1) and its contour along the lower portion of the inner wall is cut off. Consequently, large-area electrically insulated substrate (1) set on the flat surface of lower casting element (7) is kept free of gaps between lower casting element (7) and the wall of cut-off portion (6A) of upper casting element (6). In this state, the UV-curable resin with composition in the aforementioned example (not shown in the figure) is injected into upper casting element (6), followed by vacuum defoaming. Then, as shown in Figure 6(B), with pressing surface (8B1) of pressing portion (8B) on the lower side, pressing portion (8B) of casting element (8) is pressed into said casting element (6), and ridges (8B2) with V-shaped cross sections are held as they reach the surface of large-area electrically insulated substrate (1) (Figure 7). In this state, UV light is irradiated from above press-casting element (8).

When grid-shaped ridges (8B2) have a height of about 1.5 mm, and the thickness of sealing resin (5) is about 1.5 mm, as radiation emitted from a metal halide lamp (120 W/cm) is irradiated from a position about 10 cm above the upper surface of sealing resin (5), good curing can be realized as the unit is fed through at a velocity of 6 m/min for 10 passes. Then, large-area electrically insulated substrate (1) is removed from the casting element, and an external force is applied to divide it along scribe lines (1C) on large-area electrically insulated substrate (1) to form resin-sealed semiconductor devices or resin sealed electronic circuit devices of very small size, small thickness, and the sealing resin extending almost vertically from the two ends of each of the individual electrically insulated substrate pieces. Compared with the conventional devices of the same type, the assembly area is smaller by a factor of 1/3-1/4, and the thickness is smaller by a factor of about 1/2. That is, the obtained semiconductor devices and electronic circuit devices are very small in size and lightweight. Also, there is no need to perform a burr removal operation for the sealing resin.

[0024]

Figure 8 illustrates an example in which large-area electrically insulated substrate (1) shown in Figure 1 is used, and semiconductor elements are mounted on the electrically insulated substrate surface with scribe lines (1C) formed on it, followed by resin sealing. In this case, press-casting element (8) with flat and narrow top portion of ridges (8B2) is used. By using said casting element (8), it is possible to obtain resin-sealed semiconductor devices or resin-sealed electronic circuit devices that are very small in size and thickness, with the sealing resin extending vertically from the end of the individual electrically insulated substrate.

[0025]

Figure 9 is a diagram illustrating the paired chip of planar type transistor appropriate for use in the aforementioned semiconductor device. This planar type transistor is composed of the following parts: n^- epitaxial layer (11) with a sufficiently low impurity concentration grown on n^+ type semiconductor substrate (10) with a high concentration of n-type impurities; p^+ epitaxial region (12) with a high concentration of p-type impurities formed in said epitaxial layer (11), n^+ -type base region (13) with a high concentration of n-type impurities formed within said semiconductor region (12), collector electrode (14) formed on the exposed surface of semiconductor substrate (10) in a hole extending at least to the surface of semiconductor substrate (10), collector bump electrode (15) formed on collector electrode (14), emitter electrode (16) formed on emitter region (12) and ohmic contact, and emitter bump electrode (17) formed on said emitter electrode, base electrode (18) consisting of base region (12) and ohmic contact, and base bump electrode (19) formed on said base electrode, and metal film (20) for

reducing resistance in the lateral direction. This planar type transistor is characterized by the fact that collector bump electrode (15), emitter bump electrode (17) and base bump electrode (19) are all on the same plane, and their heights are all at the same level.

[0026]

As shown in Figure 1, the electroconductive pattern of electrically insulated substrate (1) is printed beforehand such that the positions of collector electrode (15), emitter bump electrode (17) and base bump electrode (19) are aligned. By means of solder cream, collector bump electrode (15), emitter bump electrode (17) and base bump electrode (19) are fixed to the electroconductive pattern. As a result, there is no need to perform wire bonding, so that it is possible to avoid all of the problems related to wire bonding. By using diodes, FETs, thyristors, resistors, capacitors, and other parts having electrodes all on one principal surface, it is possible to series-produce small, thin, resin-sealed semiconductor devices, power sources, and other electronic circuit devices without wire-bonding. Also, it is not a necessity to form scribe lines (1C) on the inner surface of electrically insulated substrate (1) such that they surround the units of each electroconductive pattern (1A). It is also possible to form scribe lines with plural electroconductive patterns (1A) integrated to form each unit. Also, one may make use of multi-layer substrates with desired circuit patterns and electroconductive patterns formed on electrically insulated substrates, and have [illegible] and holes formed on electrically insulated substrates to improve attachment of the sealing resin.

[0027]

Effects of the invention

As explained above, according to the present invention, it is possible to easily series-produce resin-sealed semiconductor devices as well as small power sources and other very small, thin, and lightweight electronic circuit devices, without the need for removal of burrs, and at a low cost, by means of simple and inexpensive equipment.

Brief description of the figures

Figure 1 is a diagram illustrating an application example of the present invention.

Figure 2 is a diagram explaining an application example of the present invention.

Figure 3 is a diagram illustrating an application example of the present invention.

Figure 4 is a diagram explaining an application example of the present invention.

Figure 5 is a diagram illustrating an application example of the present invention.

Figure 6 is a diagram illustrating an application example of the present invention.

Figure 7 is a diagram illustrating an application example of the present invention.

Figure 8 is a diagram illustrating an application example of the present invention.

Figure 9 is a diagram illustrating the semiconductor device used in the present invention.

Figure 10 is a diagram illustrating an example of the prior art.

Figure 11 is a diagram illustrating an example of the prior art.

Brief description of the part numbers

1	Electrically insulated substrate
1A	Electroconductive pattern
1B	Electrode pattern
1C	Scribe line
2	Semiconductor element
3	Solder layer
4	Metal wire
5	Sealing resin
6	Upper casting element
7	Lower casting element
8	Press-casting element
10	Semiconductor substrate
11	Epitaxial layer
12	Emitter region
13	Base region

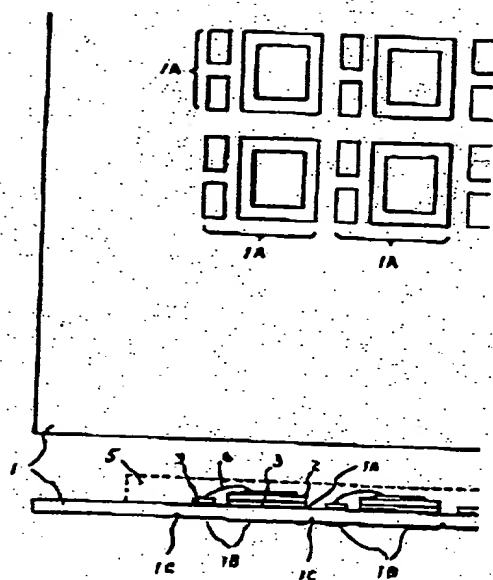


Figure 1

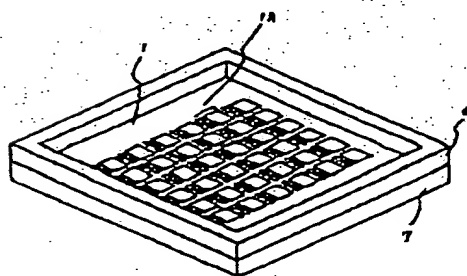


Figure 2

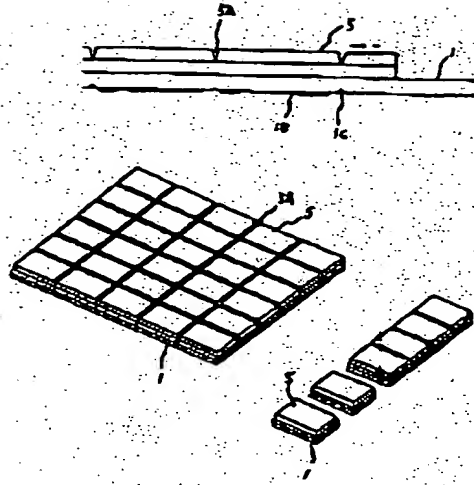


Figure 3

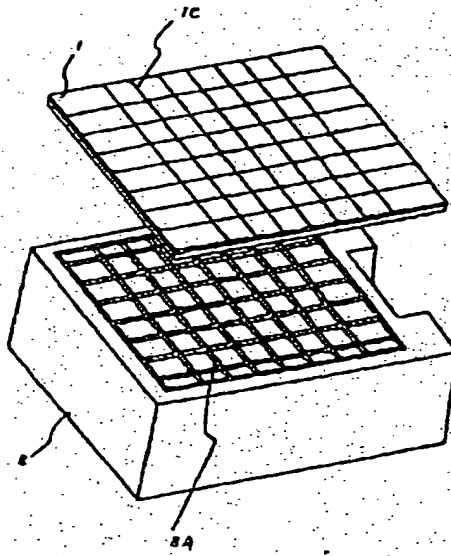


Figure 4



Figure 5

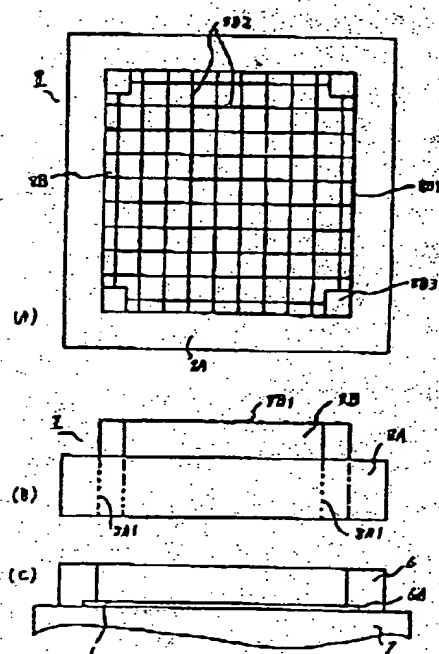


Figure 6

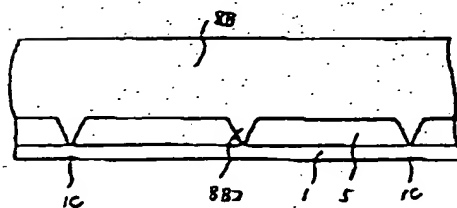


Figure 7

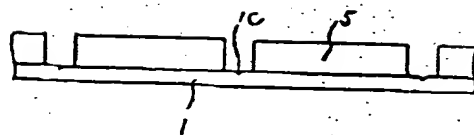


Figure 8

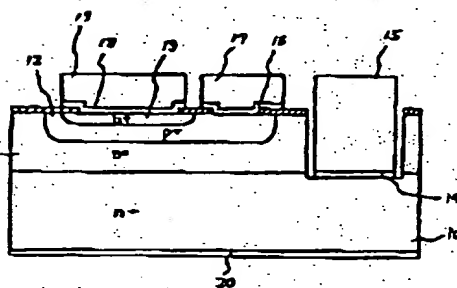


Figure 9

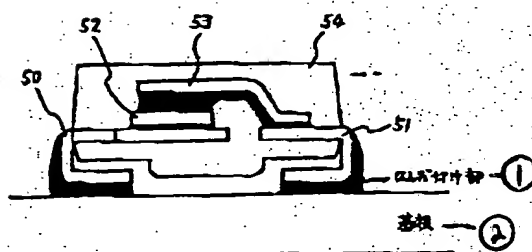


Figure 10

Key: 1 Solder layer
2 Substrate

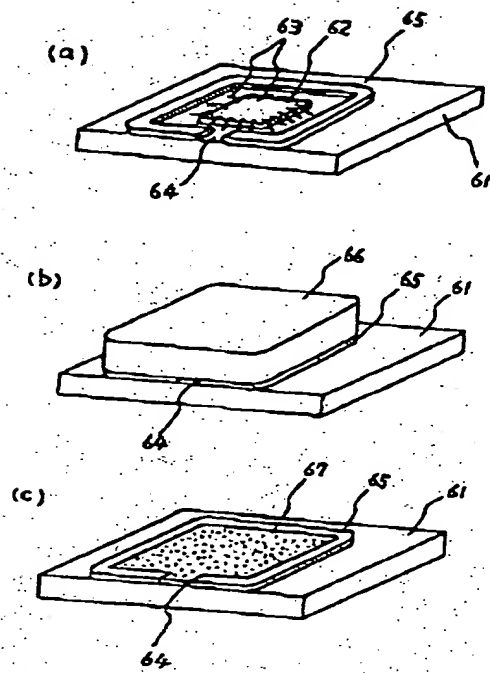


Figure 11